UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,195	12/15/2003	Kwun Yao Ho	025796-00014	4785

7590 09/14/2005

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 400
1050 Connecticut Avenue
Washington, DC 20036-5339

EXAMINER	
BRYANT, DELORIS S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/734,195	HO ET AL.	
	Examiner	Art Unit	
	Deloris Bryant	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *13-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-12* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the MCM connected with a circuit board on said third surface must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the third and fourth surfaces mentioned in claim 1 need to be included in the specification.

Claim Objections

Claim 3 is objected to because of the following informalities: applicant's units in this claim need to be corrected to either "micron" or "micrometer". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what is meant by "multichip module structure according to claim 1, wherein said chips comprise a first active chip mounted on said first multichip module substrate by flip-chip type, and at least one chip electrically connecting and stacking on a backside of a first active chip". Clarification is needed as to how the multichip module structure of claim 1, which is the first multichip module structure, is mounted on itself.

Claim 8 also recites the limitation of two "a first active chip" in lines 2 and 4. There needs to be a distinction as to whether there is one first active chip or a first and second active chip.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-3, 7 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayasaka et al.

Hayasaka et al discloses a multichip module structure, at least comprising: a first multichip module substrate, comprising: an semiconductor substrate (fig.4; 2) having a first surface and a second surface (fig. 4, "top" and "bottom" of chip 1b, respectively); an insulating layer (fig. 7A; 11) being on said first surface; a multilayer interconnection structure (fig. 4; 3) being on said insulating layer (fig. 7A; 11) and having a third surface having a plurality of first bonding pads and a fourth surface having a plurality of second bonding pads (col. 10, lns 8-18) and contacting said insulating layer(fig. 7A; 11); a plurality of conductive plugs (fig. 4; 4) penetrating said semiconductor substrate (fig.4; 2) and said insulating layer and electrically connecting to said second bonding pads (fig. 4; 6) respectively; a plurality of third bonding pads (fig. 4; bottom surface of 4) being on said second surface and connecting to said conductive plugs(fig. 4; 4)

respectively; and a plurality of chips (fig. 33; 151_1, 151_2) being on said second surface and electrically connecting to said third bonding pads.

Regarding claim 2, Hayasaka et al discloses a multilayer interconnection structure includes at least one integrated circuit device (col. 9 – col. 10, line 67 and lns 1-2, respectively).

Regarding claim 3, Hayasaka et al discloses that the hole in the silicon substrate is 100 μm (col. 12, lns 27-30), which indicated that the thickness of the substrate is at least 100 μm thick which falls within the range indicated by the applicant.

Regarding claim 7, Hayasaka et al shows the multichip module structure according to claim 1, wherein said chips individually and electrically connect to said third bonding pads (see fig. 5).

Regarding claim 11, Hayasaka el al discloses that multiple structures can be of the same structure (col. 11, lns 11-13; see fig. 4 and 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 4, 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayasaka et al in view of Ku.

Hayasaka et al discloses the claimed invention as set forth above with respect to claim 1. Hayasaka et al discloses a plurality of chips (see fig. 33). However, Hayasaka et al does not disclose the type of chips. Ku teaches that a multichip module includes a passive and active chip (col. 2, lns 16-18). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to provide an active and passive chip to be included in the multichip module structure. One would have been motivated to so modify Hayasaka et al with the passive and active chips from Ku for the benefit of using a much less costly technique (col. 1, lns 62-67).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayasaka et al in view of Ku and Taniguchi et al. Ku teaches the use of passive and active chips (col. 2, lns 8-12). Taniguchi et al teaches a flip-chip mounting process (col. 1, lns 41-51). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the flip-chip mounting process of Taniguchi et al with the passive and active chips from Ku. One would have been motivated to so modify Hayasaka et al so that connecting reliability can be ensured (col. 2, line 50).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayasaka et al in view of Taniguchi et al. Hayasaka et al discloses the claimed invention as set forth above with respect to claim 1. Hayasaka et al, however, does not disclose the multichip module connected to a circuit board. Taniguchi et al teaches that a multichip module can be mounted on a circuit board (col. 1, lns 47-48). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to take the multichip module of Hayasaka et al and mount it on a circuit board as taught by Taniguchi et al. One would have been motivated to so modify Hayasaka et al so that connecting reliability can be ensured (col. 1, lns 49-50).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Deloris Bryant whose telephone number is (571) 272-0237. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dsb

GEORGE ECKERT
PRIMARY EXAMINER